What is claimed is:

1. A capacitor comprising:

a semiconductor substrate;

a bottom conductive pattern formed on the semiconductor substrate;

a first insulating layer formed on the bottom conductive pattern;

a first metal plate formed on the first insulating layer within a first area, the first metal plate being electrically connected to the bottom conductive pattern;

a second insulating layer formed on the first metal plate;

a second metal plate formed on the second insulating layer within the first area, the second metal plate having an opening in the center thereof;

a third insulating layer formed on the second metal plate;

a third metal plate formed on the third insulating layer; and

a connecting pattern formed through the second and third insulating layers and the opening of the second metal plate, the connecting pattern electrically connecting the first and the third metal plate.

2. A capacitor according to claim 1, wherein the bottom conductive pattern is made of polysilicon.

3. A capacitor according to claim 1, wherein an area

of the first metal plate is larger than that of the second metal plate.

4. A capacitor according to claim 1, wherein an area of the third metal plate is larger than that of the second metal plate.

5. A capacitor array comprising:

a semiconductor substrate;

a bottom conductive pattern formed on the semiconductor substrate;

a first insulating layer formed on the bottom conductive pattern;

a plurality of first metal plates formed on the first insulating layer, the first metal plates being electrically connected to the bottom conductive pattern;

a second insulating layer formed on the first metal plates;

a plurality of second metal plates each of which is formed on the second insulating layer over the corresponding first metal plates, each of the second metal plates having a rectangular pattern with an opening in the center thereof and a plurality of connecting blanch patterns extending from the rectangular pattern;

a third insulating layer formed on the second metal plates;

a plurality of third metal plates each of which is formed on the third insulating layer over the corresponding second

metal palates; and

a plurality of connecting pattern formed through the second and third insulating layers and the openings of the second metal plates, the connecting patterns electrically connecting the corresponding first and third metal plates.

6. A capacitor array according to claim 5, wherein the bottom conductive patterns are made of polysilicon.

7. A capacitor array according to claim 5, wherein an area of each of the first metal plates is larger than that of each of the second metal plates.

8. A capacitor array according to claim 5, wherein an area of each of the third metal plates is larger than that of each of the second metal plates.

9. A capacitor array according to claim 5, wherein the connecting blanch patterns are connected each other to form a connecting second plate pattern including a plurality of second metal plates.

10. A capacitor array according to claim 5, wherein each of the second metal plates has four blanch patterns each of which extends from the rectangular pattern with an angle of 90 degrees.

11. A capacitor array according to claim 5, wherein the bottom conductive pattern has a plurality of conductive patterns extending to the same direction.

12. A capacitor array comprising:

a semiconductor substrate;

a bottom conductive pattern formed on the semiconductor substrate;

a first insulating layer formed on the bottom conductive pattern;

a plurality of first metal plates formed on the first insulating layer, the first metal plates being electrically connected to the bottom conductive pattern;

a second insulating layer formed on the first metal plates;

a plurality of second metal plates each of which is formed on the second insulating layer over the corresponding first metal plates, the second metal plates including,

a plurality of non-divided second metal plates each of which has a rectangular pattern with an opening in the center thereof and a plurality of first connecting blanch patterns extending from the rectangular pattern, and

a divided second metal plate having a plurality of divided patterns, a plurality of second connecting blanch patterns each of which extends from the divided pattern and a connection pattern for connecting the non-divided second metal palates;

a third insulating layer formed on the second metal plates;

a plurality of third metal plates each of which is formed

on the third insulating layer over the corresponding second metal palates; and

a plurality of connecting pattern formed through the second and third insulating layers and the openings of the non-divided second metal plates, the connecting patterns electrically connecting the corresponding first and third metal plates.

13. A capacitor array according to claim 12, wherein the bottom conductive patterns are made of polysilicon.

14. A capacitor array according to claim 12, wherein an area of each of the first metal plates is larger than that of each of the second metal plates.

15. A capacitor array according to claim 12, wherein an area of each of the third metal plates is larger than that of each of the second metal plates.

16. A capacitor array according to claim 12, wherein the first and second connecting blanch patterns are connected each other to form a connecting second plate pattern including a plurality of second metal plates.

17. A capacitor array according to claim 12, wherein each of the non-divided second metal plates has four blanch patterns each of which extends from the rectangular pattern with an angle of 90 degrees.

18. A capacitor array according to claim 12, wherein the bottom conductive pattern has a plurality of conductive patterns extending to the same direction.